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# Bi-MOSFET Amplifier for Integration with Multimicroelectrode Array for Extracellular Neuronal Recording

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**SUMMARY** A high-gain, low-noise amplifier for microelectrode probe, which integrated multimicroelectrode array for extracellular recording of neural activities and solid state circuits for the amplification of induced signals from the electrodes onto one substrate, was fabricated. In the amplifier, low-noise MOSFETs are used in the first stage, an interstage high-pass filter is incorporated to avoid saturation of the amplifier due to the polarization voltage of the electrode. In the second stage, an operational amplifier incorporating Bi-MOSFETs for the realization of high input impedance and large gain-bandwidth product is used. The gain of the fabricated amplifier is 56 dB for the frequency range between 2 Hz to 10 kHz, the noise voltage is 20 $\mu V_{pp}$; these satisfied design specifications.

***key words:*** *MOSFET, 1/f noise, microelectrode, extracellular recording, low noise amplifier*

## 1. Introduction

Neurons are concentrated locally in the central nervous system where the hierarchical information processing mechanisms are located. Here, signals are processed simultaneously, spatially and timewise with respect to the many groups of neurons. In the analysis of functions of complex nervous systems, the simultaneous analysis of neuronal impulses generated from neighboring groups of neurons and neuronal bundles at many locations is essential.

With conventional metal microelectrodes used for extracellular recording, the tip of a tungsten wire or stainless steel wire is electrolytically polished, and the other sections are insulated [1], [2]. These electrodes are fabricated easily and are effective for recording action potentials from a single neuron, but cannot be used for simultaneous recording from neighboring neuron groups. Furthermore, it is difficult to produce electrodes with the same level of impedance.

In order to solve these problems, multimicroelectrodes for extracellular simultaneous recording of neural activities have been fabricated using semiconductor microfabrication technology [3]-[12]. Since the action potentials recorded by these microelectrodes are small (100 $\mu V_{pp}$ to 300 $\mu$Vpp), the detected signals are amplified on the electrode probe and sent from the electrode; integrated multimicroelecrodes which are incorporated with solid state circuits have been fabricated [13]-[15]. Characteristics of these integrated electrodes are as follows.

(1) The shape of electrodes, arrangement and area of recording site are accurately reproduced by photolithography, and fabrication of multielectrodes is possible.
(2) Microelectrodes with high impedance and an amplifier can be fabricated on the same silicon substrate, hence electrical interference from other electrodes and the external environment can be greatly reduced with respect to recording signals from microelectrodes. This enables recording outside a shielded room.
(3) Not only can conversion of output impedance and amplification be realized on the electrode probe, but signal processing such as multiplexing is also possible.
(4) These electrodes can be utilized as stimulus electrodes, hence electronic circuits for this purpose can be integrated on a probe.

Features of amplifier for recording the potential arising from neural activities using microelectrodes must include the followings.

(1) High input impedance is required to accommodate the high impedance of the signal source through a microelectrode.
(2) The amplifier must be a low-noise type enabling amplification of neuronal impulse signals of up to approximately 100 $\mu V_{pp}$ with good $S/N$ ratio.
(3) The amplifier must have a frequency bandwidth of 10 Hz to 10 kHz which permits the recording of neuronal impulse signals without distortion.
(4) The fabrication processes for microelectrodes and integrated circuits on the same chip must be compatible.

In the present study, we designed and fabricated an amplifier circuit incorporating high-gain, low-noise silicon gate Bi-MOSFETs for integrated multimicroelectrodes, on the basis of the above-mentioned factors.

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## 2. Structure of Integrated Multimicroelectrode

Figure 1 shows the structure of the integrated electrode probe, onto which microelectrodes and an amplifier circuit are fabricated. The supporting carrier of the electrode and electronic circuit are integrated onto a single silicon crystal substrate. Action potentials of neurons are recorded at the tip of the electrode coated with thin gold; the rest of the electrode is covered with a layer of insulation. The other end of the electrode is connected to the input stage of the amplifier on the root of the electrode probe. Polysilicon, the material used for the gate electrode of the MOSFET in the amplifier circuit, is also used for the microelectrode. Through the use of $SiO_2$ and $Si_3N_4$ film for insulation, compatibility with the high temperature process during integrated circuit fabrication has been realized. The

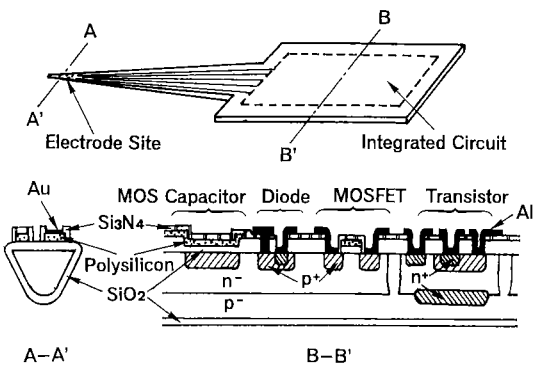


**Fig. 1** Structure of integrated elctrode probe.

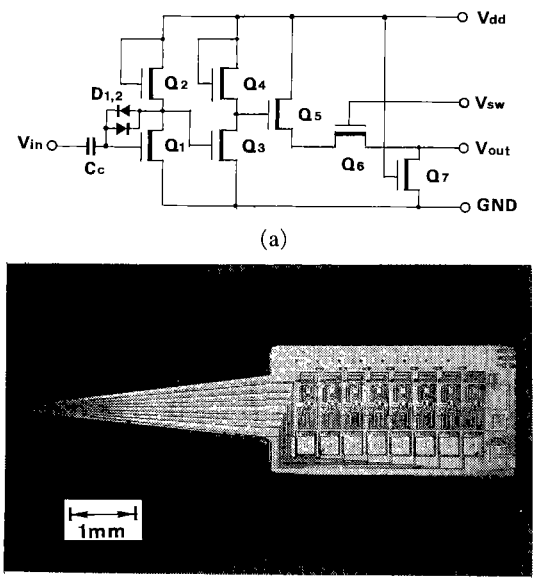


**Fig. 2** Integrated multimicroelectrode fabricated on the first design, (a) amplifier circuit using p-channel MOSFETs, (b) photomicrograph of integrated multimicroelectrode probe consisting of 8 channels.

electrode carrier was shaped through the use of anisotropic etchant after the completion of the fabrication of the integrated circuits and electrode.

The first design of the amplifier circuit is a two-stage amplifier consisting of p-channel silicon gate MOSFETs, as shown in Fig. 2(a) [13]. For the elimination of polarization voltage, *ac* coupling is adopted and an automatic bias circuit using a diode is incorporated. The problems with this circuit are that the level of integration is low due to the requirement of a large area for the capacitor at the input stage. Also, since the electrode impedance and the capacitance are connected in series with the input impedance of the MOSFETs, the signal voltages are divided and attenuated, and the $S/N$ ratio is degraded. Furthermore, since the amplification factor is approximately 20, the signal level is too small for time-division multiplexing on a probe using an analog switch.

A fabricated 8-channel multimicroelectrode probe integrated with amplifiers of the first design is shown in Fig. 2(b).

## 3. Interface Considerations

In order to obtain clear extracellular recordings of the central nervous system, microelectrodes whose impedance is around 1 Mohms to 10 Mohms (at 1 kHz) are used [15]. Figure 3 shows an equivalent circuit of the microelectrode and amplifier. The electrode impedance is represented by the resistance ($R_e$) and the capacitance ($C_e$). $Z_i$ is the input impedance of the amplifier. $C_s$ represents the shunt capacitance of the polysilicon interconnect to the silicon substrate and the surrounding fluid. $C_s$ is about 1 pF. The spreading resistance and the interconnect lead resistance are neglected.

When gold is used as the material for the electrode site, $C_e$ is essentially constant (approximately 3 $\mu Fcm^{-2}$) and independent of frequency. The value of resistance decreases in inverse proportion to the frequency (10 ohm $cm^{-2}$ at 1 kHz) [16]. This indicates that the impedance is reactive in nature. For the gold electrode whose impedance at 1 kHz is 10 Mohms, the capacitance is approximately 16 pF and the area of the electrode site is approximately 100 $\mu m^2$.

Accordingly, MOSFETs are suitable as the input stage of the amplification circuit connected to the

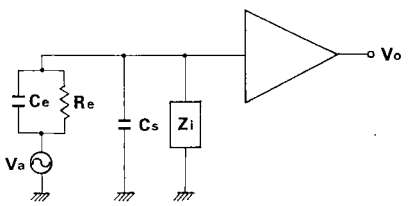


**Fig. 3** Equivalent circuit of microelectrode and amplifier.

microelectrode which has capacitive impedance. Another merit of MOSFETs is that no shot noise is produced by bias current. In an MOSFET amplifier, $Z_i$ represents a capacitance (gate input capacitance: $C_i$). At the input of the amplifier, neural action potentials ($V_a$) are decreased by a factor of $C_e/(C_e+C_i+C_s)$. The condition $C_e > C_i + C_s$ is essential to avoid degradation of the $S/N$ ratio at the input stage.

## 4. Design of Amplifier

Figure 4 shows the improved design of the amplifier circuit for the microelectrode. The circuit consists of two stages: the first-stage consists of one differential amplifier and a high-pass filter, and the second-stage amplifier consists of an operational amplifier circuit with a feedback circuit.

### 4. 1 Input Stage of Amplifier

The amplitude of neural action potentials are 100 $\mu V_{pp}$ at most. To discriminate it from noise, the noise voltage must be less than 50 $\mu V_{pp}$. Input-referred design noise voltage of the first amplifier is set at 30 $\mu V_{pp}$ for 10 Hz to 10 kHz as a typical noise voltage value. Although the input stage amplifier noise is caused by the input and the load MOSFET, the noise produced by the load MOSFET can be neglected and the only noise source is the input MOSFET when the ratio of the channel length is large enough [17].

If the noise characteristics of the first-stage MOSFET have those of $1/f$ for the frequency band, in order to satisfy the above set value, the noise level against frequency must be less than 60 $nV/Hz^{1/2}$ at 280 Hz, assuming the peak factor is 4 and the input stage consists of a differential amplifier. When the electrode capacitance is 16 pF, as described above, and the signal attenuation ratio is set to be more than 0.7 at the input stage, it is necessary that $C_i$ is less than 6 pF assuming $C_s$ is 1 pF. In order to obtain the same $S/N$ ratio as that before signal attenuation, noise voltage of the input MOSFET must be less than 42 $nV/Hz^{1/2}$ at 280 Hz, or less than 21 $\mu V_{pp}$ for 10 Hz to 10 kHz.

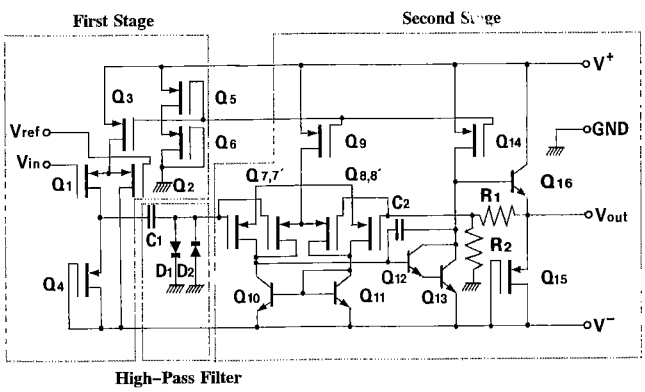


**Fig. 4** Design of Bi-MOSFET amplifier for microelectrode.

Consideration must be given to two other issues at the input stage. One of them is that the bias voltage to the MOSFET must not be applied to the electrode directly. This can be realized by introducing a differential amplifier to the first stage and connecting one of the input terminals to the reference electrode. As for the second issue, when using noble metal electrodes such as gold whose polarization potential is high, and when the amplification factor of the amplifier is large, saturation develops during operation. To avoid saturation, the first stage is constructed as a single-stage amplifier with the gain of 10, which is determined by the ratio of the channel dimension of the input and the load MOSFET. Also, the design load capacitance is set to 4 pF, and the operating current is set to 100 $\mu$A. The high cut-off frequency of the first stage was set to 19 kHz.

### 4. 2 Geometry of Input MOSFET

The magnitude of MOSFET noise greatly depends on the condition of the interface between $SiO_2$ and Si, which is affected by the silicon material and fabrication process. Noise voltages of PMOSFETs are smaller than those of NMOSFETs [18], [19], hence the circuit was designed using PMOSFETs.

A method to reduce MOSFET noise, such as chopper stabilization, cannot be used. The reason is as follows. When a MOSFET switch for chopping is installed between the gate of the input stage and the microelectrode with a capacitive source impedance, the drain or source potential of the switch floats and leak currents caused by clock feedthrough stimulate neural tissue through the microelectrode. An effective method without a circuit technique is to utilize the geometric dimensions of the gate.

Katto [20] obtained a practical relationship between the input-referred noise voltage of the MOSFET ($V_n$) and the gate size:

$$V_n^2/\Delta f = q^2 N_{Te} d_o^2/\varepsilon_o^2 L\, Wf,$$

where $d_o$: thickness of gate insulator, $L$: gate length, $W$: gate width, $N_{Te}$: effective noise trap density. This equation shows that reduction of noise of MOSFETs can be effectively accomplished by increasing the gate area ($L\,W$) and/or reducing the thickness of the gate insulator ($d_o$).

Figure 5 shows input-referred noise voltage of the P-channel silicon gate MOSFETs with different gate areas at constant $W/L$ of 10 at 280 Hz and the isoplethes of the input capacitance ($C_i$). The overlap capacitances of gate-to-source and gate-to-drain are neglected. The noise voltage was measured under the short-circuit condition of the MOSFET gates. It is not necessary to consider shot noise because no bias current exists in the MOSFET gates. The gate insulation

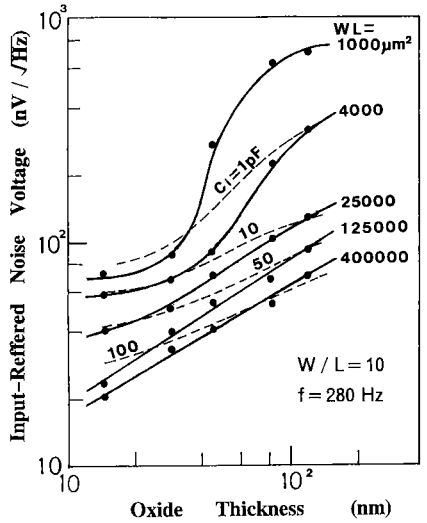


**Fig. 5** Expermentally observed input-referred noise voltage of PMOSFETs having different gate areas and a same channel ratio ( $W/L$).

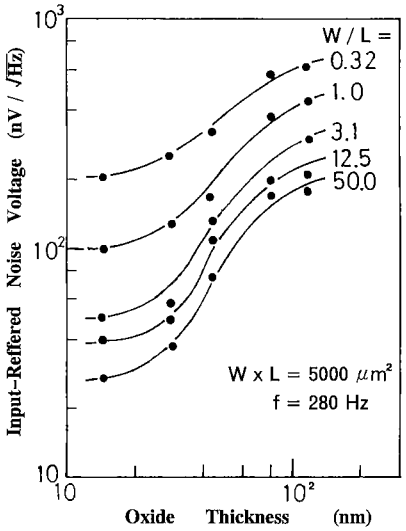


**Fig. 6** Expermentally observed input-referred noise voltage of PMOSFETs having different channel ratios ( $W/L$) and a same gate area.

film is 14 to 118-nm-thick $SiO_2$ grown by means of dry oxidation at 1100 °C. The gate area is $10^3$ $\mu m^2$ to $4\times 10^5$ $\mu m^2$.

Noise voltage is inversely proportional to the film thickness at the gate area of 1000 $\mu m^2$ ($L=10$ $\mu m$) for the thickness between 30 nm and 800 nm. For the gate area larger than 25000 $\mu m^2$ ($L=50$ $\mu m$), the noise level is inversely proportional to the 1/2 power of film thickness. Nevertheless, the MOSFETs with the gate geometry shown in this figure cannot satisfy both the conditions of noise voltage of less than 42 $nV/Hz^{1/2}$ and input capacitance of less than 6 pF. It is necessary to reduce noise voltage by modifying these gate geometries without increasing the input capacitance.

Figure 6 shows input-referred noise voltage of the MOSFETs having different $W/Ls$ at constant gate area (5000 $\mu m^2$). The magnitude of noise decreases with the increase of $W/L$ under the condition of constant gate capacitance. When $W/L$ is larger than 3.1 ($L=40$ $\mu m$) and the thickness of the film is between 30 nm and 800 nm, the magnitude of noise decreases approximately in proportion to the square of the film thickness. This approach can reduce noise voltage without increasing the input capacitance.

The noise voltage and the input capacitance of the MOSFET with $W/L$ of 50 and $d_o$ of 30 nm are 38 $nV/Hz^{1/2}$ and 5.8 pF, respectively. If the overlap capacitance and the mirror effect are neglected, this performance can satisfy the specification of the input stage of the amplifier. From these results, the input MOSFET was designed using these gate dimensions.

### 4. 3 High-Pass Filter

The high-pass filter in the intermediate stage is inserted to block the dc components from the offset voltage and polarization voltage, and to create ac coupling with the following stage. In order to set the low cutoff frequency of the filter at 10 Hz, since the upper limit of the capacitance which can be produced on the integrated circuit is 20 pF to 30 pF, the required resistance is 200 Mohms to 300 Mohms. This cannot be realized by a regular resistor. Here, incremental resistance by means of a diode was utilized. Although the magnitude of resistance created by the diode depends on the amplitude of voltage applied to it, the output signal amplitude from the first stage is less than 10 mV, and incremental resistance of 200 Mohms to 300 Mohms can easily be obtained.

### 4. 4 Second Stage

The gain bandwidth product of the second stage must be more than 10 MHz to obtain the output signal amplitude of more than 1 $V_{pp}$ at 10 kHz when the signal level at the input of the second stage is 1 $mV_{pp}$. A Bi-MOSFET operational amplifier can accomplish this performance more easily than a NMOSFET or CMOSFET. High input impedance of MOSFETs used in the input stage accommodates the large value of incremental resistance of the diode in the high-pass filter.

For the reduction of offset voltage generated in the input stage, MOSFETs in the differential input stage were divided into two sets, and geometrically symmetric arrangements have been adopted. The output signals from this amplifier, along with signals from other channels, are time-division-multiplexed by means of a multiplexing circuit on the electrode probe, and are output from the electrode probe through a buffer amplifier; therefore, the output stage of the second stage is a simple emitter follower circuit.

The open-loop gain of this circuit is approximately 120 dB, the bandwidth for the gain is 10 MHz. Accordingly, amplification of 60 dB is possible at 10 kHz. To decrease the number of wiring pads on the electrode probe, the amplification factor is not set externally, instead, a feedback resistor is installed inside the chip. The amplification factor can be adjusted by altering the wiring pattern. In the circuit used here, an amplification factor of 40 dB was selected.

## 5. Fabrication Process

As a substrate, ⟨100⟩, 10-ohm cm, p-type silicon was used. After completion of epitaxial growth for bipolar transistors, diffusion of base, drain and source was performed using boron. After diffusion of the emitter, the growth of gate oxide film (30 nm) was performed by oxidation with hydrochloric acid at 1050°C. Polysilicon doped with phosphorous was grown by means of CVD, and was used as gate electrodes.
Figure 7 shows a fabricated amplifier chip. Since an input coupling capacitor is not included, the chip area of the input stage is about half that of the first design shown in Fig. 2(b).

## 6. Electric Characteristics

Figure 8 shows the frequency characteristics of the first and second stages of the fabricated amplifier. Figure 9 shows the overall frequency characteristics of the amplifier. The amplification factor of the first stage is 18 dB and the high cutoff frequency is 35 kHz. The amplification factor of the second stage is 38 dB and the high cutoff frequency is 270 kHz. The overall amplification factor of the amplifier is 56 dB, the low cutoff frequency is 2 Hz and the high cutoff frequency is 10 kHz. The results show that the designed characteristics for both the amplification factor and frequency bandwidth have been obtained; however, the high cutoff frequency is higher than the designed value for the second stage.

Figure 10 shows noise voltage waveforms under the short-circuit condition of input terminals. The amplitude of the input-referred noise voltage is approximately 20 $\mu V_{pp}$; this satisfies the design value.

## 7. Conclusions

In order to fabricate an integrated electrode on which microelectrodes and an amplifier are incorporated onto a silicon substrate for extracellular neuronal recording, an amplifier was designed and fabricated. The requirements for the amplifier characteristics are high input impedance, low noise voltage, high voltage gain and avoidance of a saturation state of the amplifier due to the polarization voltage of the microelectrode.

The features of the amplifier are 1) the use of

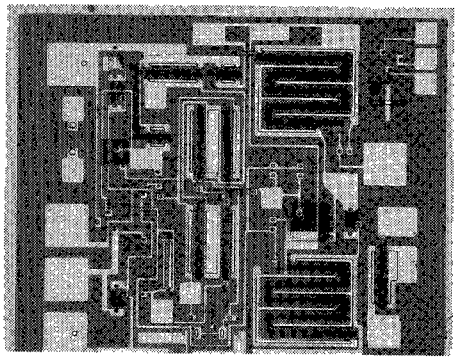

**Fig. 7** Die photomicrograph of Bi-MOSFET amplifier.

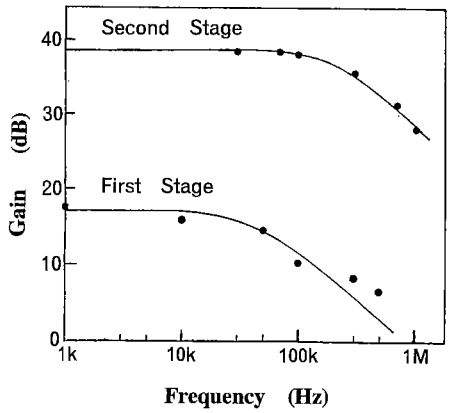


**Fig. 8** Frequency responses of the first and the second stages in the amplifier.

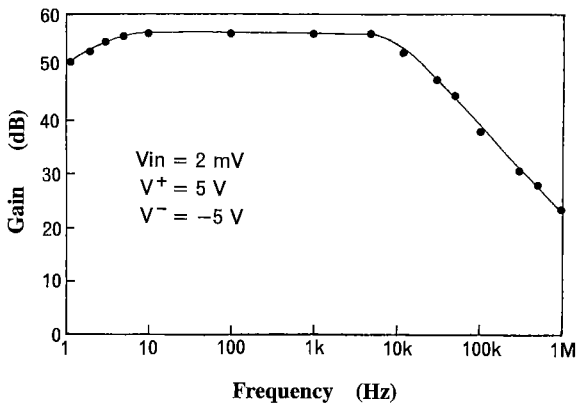


**Fig. 9** Total frequency response of amplifier.

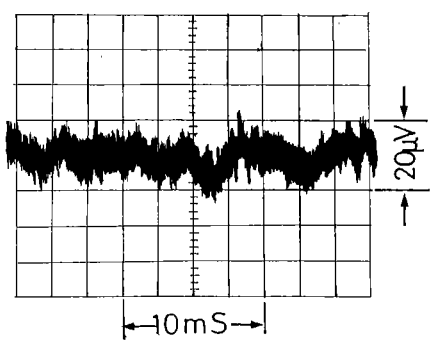


**Fig. 10** Noise voltage waveform of amplifier.

MOSFETs for the input stage, and incorporation of the noise reduction by means of the geometric effect of the gate, 2) incorporation of a high-pass filter into the integrated circuit by means of the incremental resistance of a diode and by arranging this filter between the first and second stages to construct a monolithic ac amplifier, and 3) incorporation of Bi-MOSFETs in the second stage to realize high input impedance and large gain bandwidth product.

The results of this study verify the design and the processing conditions of amplifiers in the fabrication of integrated electrodes on which multimicroelectrodes and amplifiers are incorporated.

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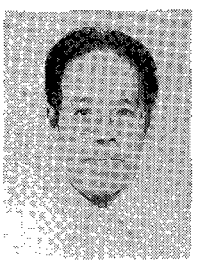

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