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A Study on the M-ary/SS Communication System Using a Frame Synchronization Method of PCM Communication Systems

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SUMMARY Synchronization has been one of the problems in M-ary spread spectrum communication systems. In this letter, we propose the frame synchronization method using the Hadamard matrix and a frame synchronization method of PCM communication systems. Moreover, we analyze the probabilities of keeping synchronous state and frame renewal rates, and we evaluate the relationship between these probabilities and the number of stages of counters.

key words: *spread spectrum communication system, M-ary/SS communication system, PCM communication system, frame synchronization method, Hadamard matrix*

1. Introduction

Spread Spectrum (SS) communication systems are resistant to interference and have a low probability of interception. M-ary Spread Spectrum (M-ary/SS) communication systems, which have more than one spreading code, can improve Bit Error Rate (BER) performance under conditions in which there is additive white Gaussian noise (AWGN) [1]–[4], [6]. The synchronization of M-ary/SS communication systems is difficult, however, because they have plural spreading codes. Much effort has therefore gone into developing appropriate synchronization methods. There is, for example, a system using several delay lock loops [2], [4] and a scheme using a synchronizing spreading code [3].

In this letter, we propose a frame synchronization method for the M-ary/SS communication systems using a Hadamard matrix and a frame synchronization method of PCM communication systems [6], [7]. The proposed method uses the row vectors of a Hadamard matrix as the spreading code. The head chip of each code is plus. Since the head chip of each code is used for frame synchronization, it is possible to implement a simple synchronization system without extra synchronizing signals. We analyze probabilities of keeping synchronous state and the frame renewal rates, and we evaluate their relation to the number of stages of counters. A way of analyzing the frame synchronization of PCM communication systems [5] is used in this analysis.

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2. Synchronization System

2.1 Hadamard Matrix

A Hadamard matrix is defined as

$$H_M = \left[\begin{array}{c|c} H_{M-1} & H_{M-1} \\ \hline H_{M-1} & \overline{H_{M-1}} \end{array}\right] \tag{1}$$

For example, when $M = 2$,

$$H_2 = \left[\begin{array}{cc|cc} + & + & + & + \\ + & - & + & - \\ \hline + & + & - & - \\ + & - & - & + \end{array}\right] = \left[\begin{array}{c} a_1 \\ a_2 \\ a_3 \\ a_4 \end{array}\right] \tag{2}$$

The row vectors $a_i (i = 1, \cdots, 4)$ of a Hadamard matrix are used as spreading code. The correlation value between any two codes becomes zero, and the head chip of every code is plus. The head chip of each code is therefore used for the frame synchronization.

2.2 Frame Synchronization Method

The proposed method uses the Hadamard matrix and a frame synchronization method of PCM communication systems [5] as shown in Fig. 1. This frame synchronization system consists of one shift register and three

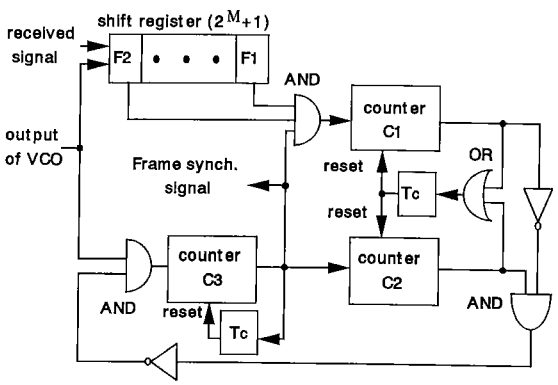

Fig. 1 Frame synchronization system.

counters (C1, C2, and C3). The output signals of the voltage-controlled oscillator (VCO) of the phase-lock loop (PLL) are used as the chip clock signals. The counter C3 counts chips up to 2^M (the length of the spreading code) and then makes a frame synchronizing signal. The counter C1 and the counter C2 are used for renewal of the synchronizing signal. When both the F1 pulse and the F2 pulse in the shift register become plus and an output state of the counter C3 is high, the counter C1 increases. That is, the counter C1 counts if the frame synchronizing signal is regarded as correct. When the counter C1 reaches m (the number of stages of counter C1), it outputs a signal to reset counters C1 and C2. The counter C2 counts the output signals of the counter C3. When the counter C2 reaches n (the number of stages of counter C2), the output signal of the counter C2 resets counters C1 and C2. Here, n is greater than m because counter C2 always resets both of the counters when $m > n$. The output signal of counter C1 resets both of the counters whenever the frame synchronizing signals are regarded as correct. When they are incorrect, the output signal of the counter C2 resets both of the counters and makes counter C3 not count one chip. Counter C3 will then be allowed to step back one chip, renewing the frame synchronizing signal.

3. Performance Evaluation

We assume an AWGN environment and complete chip synchronization. The frame synchronization is regarded as correct when the output signal of counter C1 resets counters C1 and C2. When the frame timing is correct, the probability of keeping synchronous state is (Appendix A.1):

$$P_l(m,n) = p^m \left(1 + \sum_{i=2}^{n-m} \sum_{j=1}^{[i/2]} \left\{ \binom{m+j-1}{j} (pq)^j \binom{i-j-1}{i-2j} q^{i-2j} \right\}\right), \tag{3}$$

where $p = 1 - q$, $q = \frac{1}{2} erfc(\sqrt{\frac{M}{2^M}\frac{E_b}{N_0}})$, E_b is transmitted signal energy per bit, N_0 is the noise power spectral density, and $[\cdot]$ is Gauss notation.

When the frame timing is incorrect, the frame renewal rate is (Appendix A.2):

$$P_t(m,n) = 1 - P_a(m,n) - \frac{1}{4}\{P_a(m,n-1) - P_a(m-1,n-1)\}, \tag{4}$$

where

$$P_a(m,n) = \left(\frac{1}{2}\right)^m \left(1 + \sum_{i=2}^{n-m} \sum_{j=1}^{[i/2]} \left\{ \binom{m+j-1}{j} \binom{i-j-1}{i-2j} \left(\frac{1}{2}\right)^i \right\}\right). \tag{5}$$

Calculated values of P_l and P_t versus are shown in Fig. 2 for a frame length of 16 chips, the counter C1 having 16 stages, and $E_b/N_0 = 5$ [dB]. The probability P_l is almost 1 when n is greater than 30. Therefore, the synchronizing signal is regarded as correct. According to the P_t curve, the synchronizing signal is apt to be renewed at smaller values of n. Figure 3 shows weighted average of P_l and P_t $(\alpha \cdot P_l + (1-\alpha) \cdot P_t)$ versus the number of stages of counter C2. Each curve shows the characteristic of weighted average when $\alpha = 0.2, 0.4, 0.6, 0.8$. The value of α may change in accordance with requirements of the system. The maximum point of each curve gives the optimal value for the number of stages of counters C1 and C2 under condition of those weights. Figure 3 shows that the optimal value for the number of stages of counter C2 exists from 27 to 32. Therefore, it is possible to say that the optimal value for the number of stages of counter C2 exists in the neighborhood of 30 when the frame length is 16, the counter C1 has 16 stages, and $E_b/N_0 = 5$ [dB].

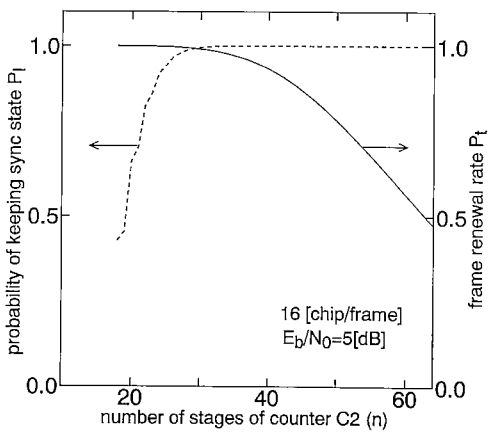

Fig. 2 Characteristic of P_l and P_t when m (the number of stages of counter C1) = 16.

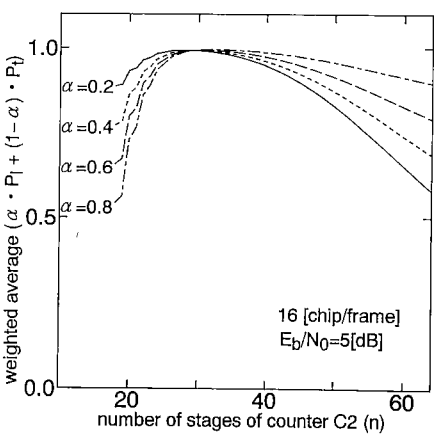

Fig. 3 Characteristic of weighted average $(\alpha \cdot P_l + (1-\alpha) \cdot P_t)$ when m (the number of stages of counter C1) = 16.

4. Conclusions

In this letter, we have proposed the frame synchronization method using the Hadamard matrix and a frame synchronization method of PCM communication systems. We have calculated the probability P_l of keeping synchronous state and the probability P_t of the frame renewal rate. Evaluating the relationship between these probabilities and the number of stages of counters, we estimated the optimal value for the number of stages of counter C2 suitably for the number of stages of counter C1. We found that there is an appropriate combination of stages of the two counters.

Future work is as follows.

- The analysis of BER performance in consideration of the synchronization.
- The analysis of acquisition time based on probability P_l and P_t.
- The analysis of chip synchronization in detail, which is assumed to be complete in this letter.
- The analysis of simulated performance using the proposed synchronization system.

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Appendix

A.1 Derivation of Expression (3)

When the frame timing is correct, behavior of the proposed synchronization system is expressed as the state transition diagram shown in Fig. A· 1. Changing the state depends on the input value of F2 and involves increasing both counters C1 and C2 or increasing only C2. Clearly, it takes at least m transitions to fill counter C1. To keep synchronous state, it is necessary to fill counter C1 before counter C2 reaches n. Therefore, the spare transitions, which are along paths labeled p2, p3, and p4, are allowed $(n-m)$ times at most. Note that:

- When we have i $(\geqq 2)$ spare transitions, the paths labeled p2 are followed once at least and $[i/2]$ times at most, where $[\cdot]$ is gauss notation.
- Moreover, when the paths labeled p2 are followed j $(\leqq [i/2])$ times, the paths labeled p3 are followed the same times and the paths labeled p4 are followed $(i-2j)$ times. Thus, F2 should get '1' j times, and get '0' $(i-j)$ times.

When j paths labeled p3 are selected from m (C1:0, ..., C1:m-1), the repeated combination is:

$$\begin{pmatrix} m+j-1 \\ j \end{pmatrix}. \tag{A·1}$$

When $(i-2j)$ paths labeled p4 are assigned to j paths labeled p3, the repeated combination is:

$$\begin{pmatrix} i-j-1 \\ i-2j \end{pmatrix}. \tag{A·2}$$

Therefore, expression (3), which is the probability of counter C1 being full before counter C2, is:

$$P_l(m,n) = p^m \left(1 + \sum_{i=2}^{n-m} \sum_{j=1}^{[i/2]} \left\{ \begin{pmatrix} m+j-1 \\ j \end{pmatrix} (pq)^j \begin{pmatrix} i-j-1 \\ i-2j \end{pmatrix} q^{i-2j} \right\} \right), \tag{A·3}$$

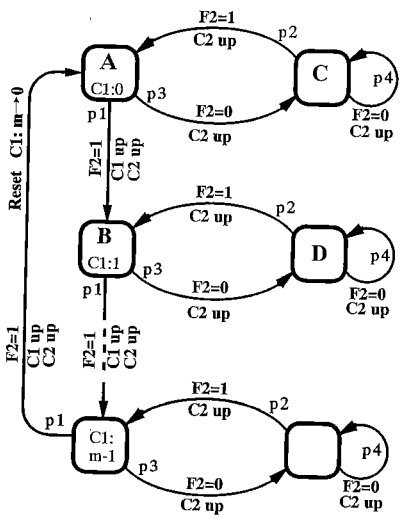

Fig. A· 1 State transition diagram of the synchronization system.

where p is the probability of F2 being 1, and q is the probability of F2 being 0.

A.2 Derivation of Expression (4), (5)

When the frame timing is incorrect, $p = q = \frac{1}{2}$. Thus, expression (5) comes from expression (3) for $p = q = \frac{1}{2}$. When counter C2 becomes full earlier than counter C1, 1 chip shift is carried out. Then the state gets to state B, C, or D. The probability of getting to state B, C, or D, and the counts of counter C1 and C2 are:

- State B probability is $\frac{1}{4}$, C1=1, and C2=1.
- State C probability is $\frac{1}{2}$, C1=0, and C2=1.
- State D probability is $\frac{1}{4}$, C1=0, and C2=1.

The probability of counter C1 being full before counter C2 starting from state B, C, or D is:

- Starting from state B $P_a(m-1, n-1)$.
- Starting from state C $\{P_a(m,n) - \frac{1}{2}P_a(m-1, n-1)\}/(\frac{1}{2})$.
- Starting from state D $P_a(m, n-1)$.

According to these probabilities, the probability of counter C1 being full earlier than counter C2 after 1 chip shift is carried out is:

$$P_b = \frac{1}{4}P_a(m-1,n-1) + \frac{1}{2}\{P_a(m,n) - \frac{1}{2}P_a(m-1,n-1)\}/(\frac{1}{2}) + \frac{1}{4}P_a(m,n-1). \quad \text{(A·4)}$$

Therefore, expression (4), which is the probability of counter C2 being full before counter C1, is:

$$1 - P_b. \quad \text{(A·5)}$$