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A Self-Synchronization Method for the SS-CSC System

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SUMMARY In this paper, a simple frame synchronization method for the SS-CSC system is proposed, and the synchronization performance is analyzed. There have been growing interests in the M-ary/SS communication system and the bi-orthogonal modulation system because these systems can achieve the high frequency utilization efficiency. However, the frame synchronization is difficult. We proposed the SS-CSC system, and evaluated the bit error rate (BER) performance of the SS-CSC system under the completed synchronization. The BER performance of the SS-CSC system is much the same as that of the bi-orthogonal modulation system. In this paper, a frame synchronization method using the differential detector and racing counters is proposed. In particular, the lose lock time, the recovery time and the BER performance considering the synchronizing performance are analyzed. In consequence, the BER performance considering the synchronization performance can approach the lower bound of the SS-CSC system by tuning the number of the stages in racing counters.

key words: *M-ary orthogonal system, bi-orthogonal system, self-synchronization, frame synchronization, differential detector, racing counters*

1. Introduction

Spread Spectrum (SS) communication systems are of considerable interest for numerous applications including mobile communication systems and power-line transmission systems. Most work done on SS communication systems has concentrated on the binary transmission of data, for example, polar signaling [1]–[3]. The bit error rate (BER) performance of the SS communication system is the same as that of the PCM communication system in Additive White Gaussian Noise (AWGN) environments.

On the other hand, M-ary Spread Spectrum communication (M-ary/SS) systems and bi-orthogonal modulation systems, which use M orthogonal codes, have been attracting increasing interest in recent years [4], [5]. The BER performance of the M-ary/SS system and the bi-orthogonal modulation system can approach Shannon's Limit by increasing the number of the spreading codes in AWGN environments. Moreover, these systems are also effective from viewpoint of frequency utilization efficiency. However, the M-ary/SS system and the bi-orthogonal modulation system have a serious problem; synchronization of these systems is very difficult because they have several spreading codes and cannot use the synchronization systems for conventional SS systems directly [6]–[10].

We proposed the spread spectrum communication system with constrained spreading code, that is, the SS-CSC system [11]–[13]. The SS-CSC system contains the conventional systems such as the direct-sequence spread spectrum (DS/SS) system, the M-ary/SS system, and the bi-orthogonal modulation system. The spectral efficiency of the SS-CSC system is better than that of the M-ary/SS system. However, the synchronization of the SS-CSC system is also difficult. The synchronization system using racing counters treated in [9], [10] is not applicable to the SS-CSC system directly because the polarity of the spreading sequence changes. So for, we investigated the synchronization method with a synchronizing spreading code for the SS-CSC system. In the synchronization system using a synchronizing spreading code [12], part of the channel capacity is occupied to transmit timing information. Thus the BER performance degrades as the energy of the synchronizing spreading code increases. It was therefore important to investigate the self-synchronization method where timing information is extracted from the received signal itself without any pilot-like signal.

In this paper, we propose a simple frame synchronization method for the SS-CSC system. In the proposed synchronization system, the timing information is extracted from the received signal itself. The proposed synchronization system consists of the differential detector and racing counters. We evaluate the recovery time, the lose lock time, and the BER performance considering the synchronization performance by theoretical analysis. Moreover, we compare the SS-CSC system with the M-ary/SS system where all of the sequences are composed by repeating the same sequence L times (L is the constraint length).

The outline of this paper is as follows. In Sect. 2, we explain the structure of the SS-CSC system and describe the proposed synchronization system with the differential detector and racing counters. In Sect. 3, we derive the recovery time, the lose lock time, and the BER performance considering the synchronization performance by theoretical analysis. In Sect. 4, we discuss

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Table 1 Notation.

Length of spreading code	M [chip]
Length of message bits to select one of M orthogonal spreading code	K [bit]
Length of message bits to modulate the selected spreading code	N [bit]
Constraint length	L [sequence]
Transmitted signal energy per message bit to Noise power spectral density ration	E_b/N_0 [dB]
recovery time	T_{recov} [frame]
lose lock time	T_{lock} [frame]
period of one spreading code	T [sec]
period of one chip	T_c [sec]
the number of the stages of the counter $C1$	m [stage]
the number of the stages of the counter $C2$	n [stage]

the numerical results. Finally, we summarize the main results in Sect. 5. Table 1 shows the notation on the following discussion.

2. System Structure

In this section, we explain the principle of the basic SS-CSC system [11] and describe the frame synchronization system with the differential detector and racing counters. Figure 1 shows the structure of the basic SS-CSC system. Figure 2 shows the proposed frame synchronization system. Figure 3 illustrates each part signal of the SS-CSC system using the differential detector and racing counters.

2.1 Principle of the SS-CSC System

The transmitter of the SS-CSC system acts as follows. Firstly, source data are converted into $\log_2(2^{K+N})$ [bit] data by the data converter. Source data are distributed into two classes, namely K [bit] data to select one of $M(=2^K)$ spreading codes $(PN_i(t), i = 1, 2, \ldots, M)$ and N [bit] data to modulate its selected spreading code. Secondly, one of M spreading codes (orthogonal codes are employed in this study) is selected by K [bit] data. Thirdly, N [bit] data, $d(t)$, is spread by the selected spreading code. Lastly, the spread signal at point (c) is multiplied by another spreading code $A(t)$, and it is transmitted. The spreading code $A(t)$ is used to improve the probability of frame timing error. The selected spreading code is constrained for period L [sequence]. Here the constraint length L is

$$L = \begin{cases} 1 & (N = 0) \\ N & (N \geq 1) \end{cases} \tag{1}$$

Therefore, the frame length is $L \times M$ $(= L \times 2^K)$ [chip]. Thus each frame conveys $\log_2(2^{K+N})$ $(= K+N)$ binary symbols.

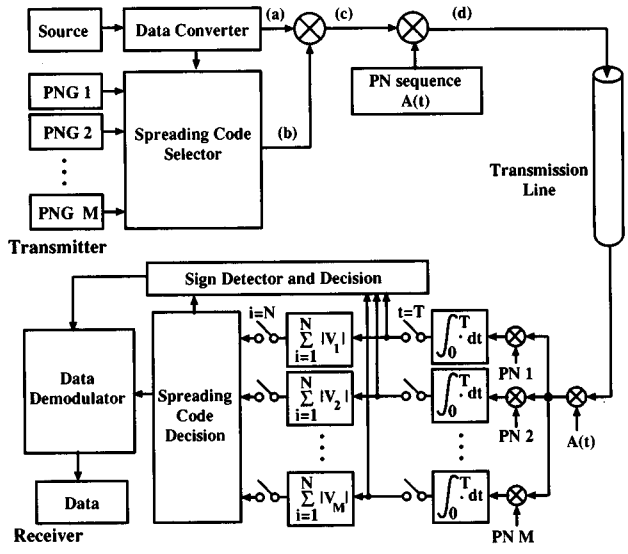

Fig. 1 Structure of the basic SS-CSC system.

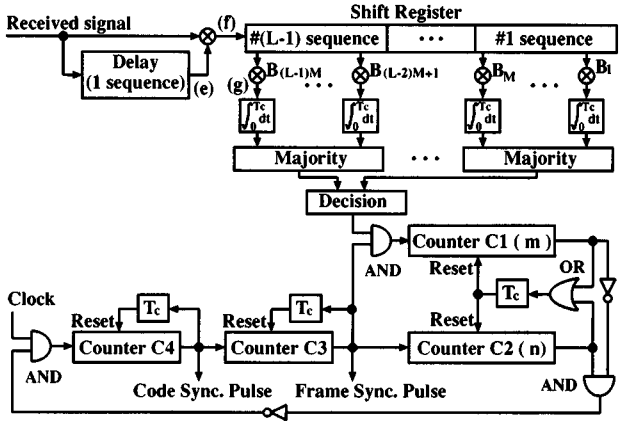

Fig. 2 Structure of the proposed frame synchronization system.

The transmitted signal $S(t)$ is expressed as

$$S(t) = \sqrt{P} d(t) \cdot PN_i(t) \cdot A(t), \tag{2}$$

where $PN_i(t)$ is the selected spreading code with period T, $A(t)$ is also spreading code with period LT, and P is the power of the transmitted signal. If a rectangular pulse is defined by $p_x(t) = 1$ for $0 \leqq t < x$ and $p_x(t) = 0$, otherwise, $d(t)$ can be expressed as $d(t) = \sum_{j=-\infty}^{\infty} d_j p_T(t - jT)$, where the sequence (d_j) is the binary data sequence $(d_j \in \{-1, 1\}$ for each $j)$. Moreover, the spreading codes $PN_i(t)$ and $A(t)$ are expressed as $PN_i(t) = \sum_{j=1}^{M} PN_j^{(i)} p_{T_c}(t - jT_c)$ and $A(t) = \sum_{j=1}^{LM} A_j p_{T_c}(t - jT_c)$, respectively, where $(PN_j^{(i)})$ and (A_j) are a periodic binary sequence of elements from the set $\{-1, 1\}$.

In the receiver, the polarity of the spreading code is demodulated after the transmitted spreading code is estimated. The K [bit] data is demodulated by estimation of the transmitted spreading code, and the N [bit]

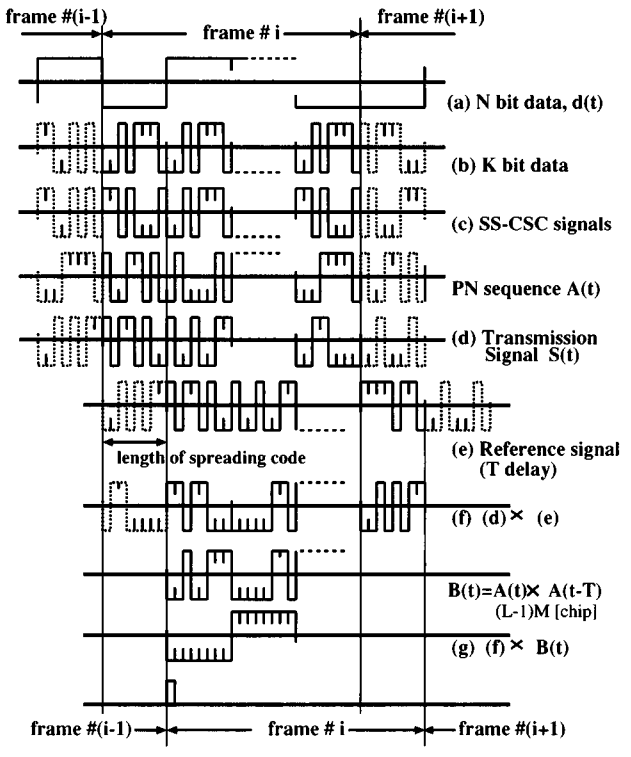

Fig. 3 Each part signal.

data is determined by polarity of the estimated spreading code. In Fig. 1, it contains M correlators, each one corresponds to one of the possible M spreading codes. Each correlator consists of a multiplier that multiplies one of the M spreading codes by the received signal and an integrator that integrates the product over the duration T. The outputs of the M correlators are all sampled at time T. These correlator outputs pass through circuits that detect the magnitude of the signal without regard to the sign similar to the conventional bi-orthogonal modulation system. And outputs of the absolute circuits input the summation circuits. These magnitudes of the summation circuit outputs are examined and the largest one is selected. Having determined which of the signals is the largest, that particular correlator output is examined again and the polarity of the signal determined at every T.

The frame timing is tracked by the proposed synchronization system as shown in Fig. 2. In next subsection, we describe the structure of the proposed synchronization system with the differential detector and racing counters.

2.2 Synchronization System

In the proposed synchronization system, it contains a differential detector, a shift register, $(L-1)$ majority circuits, a decision circuit and four counters $(C1, C2, C3, C4)$. The sub-system joining counter $C1$ to counter $C2$ is called racing counters.

The function of each component in the proposed synchronization system is as follows.

- **The differential detector** multiplies the received signal by a reference signal which delays the received signal by period of one sequence T.
- **The shift register** has $M(L-1)$ stages which correspond to $(L-1)$ sequences and stores the output of the differential detector. The stored value is correlated with $B(t)$. $B(t) = \sum_{j=1}^{(L-1)M} B_j p_{T_c}(t - jT_c)$, where (B_j), which is a periodic binary sequence of elements from the set $\{-1, 1\}$, is $A_j \times A_{j+M}$.
- **Each majority circuit** evaluates M correlation values between the stored value of the shift register and $B(t)$. If the number of correct estimated chips is not less than $3M/4$, the majority circuit outputs "+1." Otherwise, the output signal of the majority circuit obtains "−1."
- **The decision circuit** decides the sum of the majority circuit outputs. If the sum of the majority circuit outputs is not less than zero, the output signal of the decision circuit gets "+1." The output signal, otherwise, obtains "−1."
- **The counter $C1$** is used to retain the frame timing. The counter $C1$ counts when the output signal from the decision circuit and the output signal of the counter $C3$ become "+1" at the same time. When the counter $C1$ reaches m, the output signal of $C1$ resets both counter $C1$ and counter $C2$ to zero.
- **The counter $C2$** is used to renew the frame timing. The counter $C2$ counts even if the frame timing is incorrect. When the counter $C2$ reaches n, both counter $C1$ and counter $C2$ are reset to zero.
- **The counter $C3$** counts until it reaches L and makes a frame synchronization signal. When the counter $C3$ reaches L, the counter $C3$ resets itself.
- **The counter $C4$** counts until it reaches M and makes a code synchronization signal. When the counter $C4$ reaches M, the counter $C4$ resets itself.

The synchronization system operates as follows.

- **In the case of the correct synchronization**:

  The output of the decision circuit becomes "+1." Then the counter $C1$ increases its count by one. When the counter $C3$ reaches L, it outputs the frame synchronizing signal and the counter $C2$ increases its count by one. Therefore, both counter $C1$ and counter $C2$ count at the same rate. Here, we set $m < n$ so that the counter $C1$ reaches the full count earlier than the counter $C2$. When the

counter $C1$ reaches the full count, both counter $C1$ and counter $C2$ are reset to zero by resetting signal of the counter $C1$ and the frame timing is held.

- **In the case of the incorrect synchronization**:

  The output of the decision circuit becomes "-1." Then the counter $C1$ gets hard to increase. The counter $C2$ increases its count by one when the counter $C3$ reaches L. Therefore, the counter $C2$ reaches the full count earlier than the counter $C1$. When the counter $C2$ reaches the full count, both the counter $C1$ and the counter $C2$ are reset to zero by resetting signal of the counter $C2$ and the counter $C4$ is allowed to step back by a one chip interval. Thus, the renewal of the frame timing is carried out.

3. Performance Analysis

In this section, we derive the lose lock time, the recovery time, and the BER performance considering the synchronization performance by theoretical analysis. The lose lock time means the average time holding correct frame timing. The recovery time means the average time to establish synchronization after synchronization collapses. Let us assume the followings: the received signal is affected by an AWGN channel; (the noise over the received signal is independent of that over the reference signal;) the chip synchronization is established completely.

The error probability of the majority circuits output is given by

$$p' = \begin{cases} \displaystyle\sum_{i=M/4}^{3M/4} p_s^{M-i} \binom{M}{M-i} (1-p_s)^i \\ \qquad \text{for correct frame timing,} \\ \left(\frac{1}{2}\right)^M \left(\displaystyle\sum_{i=M/4}^{3M/4} \binom{M}{M-i} \right) \\ \qquad \text{for incorrect frame timing,} \end{cases} \tag{3}$$

where p_s is the correct probability of the differential detector output. The probability of the decision circuit output being "+1" is given by

$$p = \sum_{i=0}^{[L/2]} (1-p')^{L-1-i} \binom{L-1}{L-1-i} (p')^i \tag{4}$$

where [ ] is Gauss notation.

Figure 4 shows the state transition diagram of racing counters. The transition from one state to another state depends on the output of the decision circuit.

In this system, it takes at least m transitions to fill the counter $C1$. To keep the correct frame timing, it is necessary to fill the counter $C1$ before the counter $C2$ reaches n. Therefore, the spare transitions, which are along the paths labeled $R2$, are allowed $(n-m)$ times

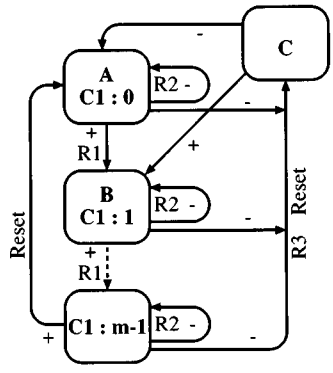

Fig. 4 State transition diagram of racing counters.

at most. If the counter $C1$ does not fill for n transition times, the transition is along the paths labeled $R3$ and the frame timing is renewed.

The holding probability of the frame timing is given by

$$P_h(m,n,p) = p^m \left(1 + \sum_{i=1}^{n-m} \binom{m+i-1}{i} q^i \right), \tag{5}$$

where p is the probability of the decision circuit output being "+1," and q is the probability of the decision circuit output being "-1," that is, $q = 1-p$.
The renewing probability of frame timing is given by

$$P_r(m,n,p) = 1 - pP_{BA}(m,n,p) + qP_{AA}(m,n,p), \tag{6}$$

where $P_{BA}(m,n,p)$ is the transition probability from state B to state A, $P_{AA}(m,n,p)$ is the transition probability from state A to state A. $P_{BA}(m,n,p)$ and $P_{AA}(m,n,p)$ are given by

$$P_{BA}(m,n,p) = P_h(m-1,n-1,p), \tag{7}$$

$$P_{AA}(m,n,p) = P_h(m,n-1,p). \tag{8}$$

Therefore, it is necessary for average transition times T_{AA} to transfer from state A to state A. T_{AA} is given by

$$T_{AA}(m,n,p) = \frac{1}{P_h(m,n,p)} \cdot \left\{ mp^m + \sum_{i=1}^{n-m} \left\{ (m+i)p^m \binom{m+i-1}{i} q^i \right\} \right\}. \tag{9}$$

Moreover, it is necessary for average transition times T_{CA} to transfer from state C to state A. T_{CA} is given by

$$T_{CA}(m,n,p) = \frac{1}{1-P_r(m,n,p)} \cdot \Big\{ 1 - P_r(m,n,p) \left(T_{AA}(m-1,n-1,p) + 1 \right)$$

$$+qP_h(m,n-1,p)\,(T_{AA}(m,n-1,p)+1)\Big\}. \tag{10}$$

Therefore, the average lose lock time is given by

$$T_{lock}=n+\Big(1-P_r(m,n,p_c)\Big)\Big\{T_{CA}(m,n,p_c)+T_{AA}(m,n,p_c)\frac{P_h(m,n,p_c)}{1-P_h(m,n,p_c)}\Big\}, \tag{11}$$

where p_c is the probability of the decision circuit output being "+1" when the frame timing is correct, $P_r(m,n,p_c)$ is the renewing probability of the correct frame timing, $T_{CA}(m,n,p_c)$ is the number of frames to transit from state C to state A under the correct frame timing, $T_{AA}(m,n,p_c)$ is the number of the average frames of the filling the counter $C1$ under the correct frame timing, and $P_h(m,n,p_c)$ is the holding probability of the correct frame timing.

The recovery time T_{recov} is given by

$$T_{recov}=\Big\{T_r(m,n,p_e)+n\Big\}\frac{P_r(m,n,p_c)}{1-P_r(m,n,p_c)}+T_r(m,n,p_e)+T_{CA}(m,n,p_c), \tag{12}$$

where p_e is the probability of decision circuit output being "+1" when the frame timing is incorrect, $T_r(m,n,p_e)$ is the number of frames taken to get back to the correct frame timing.

The BER performance considering the synchronization performance is given by

$$BER=\frac{T_{lock}P_{b1}+T_r(m,n,p_e)P_{b2}}{T_{lock}+T_r(m,n,p_e)} \tag{13}$$

where P_{b1} is the BER for the correct frame timing in [11] and P_{b2} is the BER for the incorrect frame timing, that is, 1/2.

4. Numerical Results

Figure 5 shows the lose lock time and the recovery time versus the constrained length L when $K=3$ [bit], $m=3$ [stage], $n=10$ [stage], and $E_b/N_0=8$ [dB]. The lose lock time for L =odd number is longer than that for L = even number because the decision circuit outputs "+1" when the sum of the majority circuit outputs is not less than zero. Moreover, the lose lock time is maximum value when $L=3$ [sequence]. The recovery time increases as L increases because the number of chips in a frame increases with increasing L. The recovery time is much shorter than the lose lock time.

Figure 6 shows the lose lock time when $K=3$ [bit], $N=3$ [bit], $m=3$ [stage], and $n=5$, 10, and 15 [stage]. Each line shows the theoretical value and each plot shows the computer simulation value. The lose lock time is exponentially increased as E_b/N_0 becomes large. Moreover, it is found that increasing n is effective in improvement of the lose lock time.

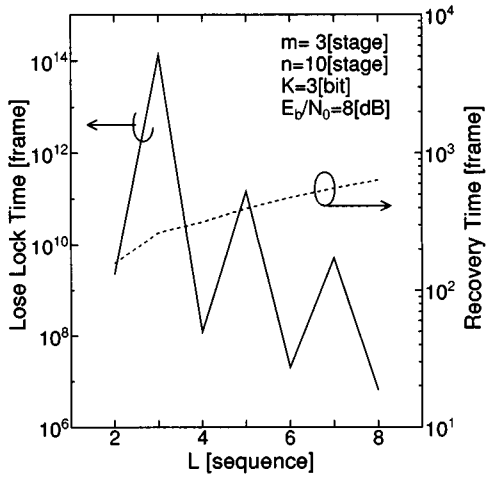

Fig. 5 Lose lock time and recovery time versus constrained length L.

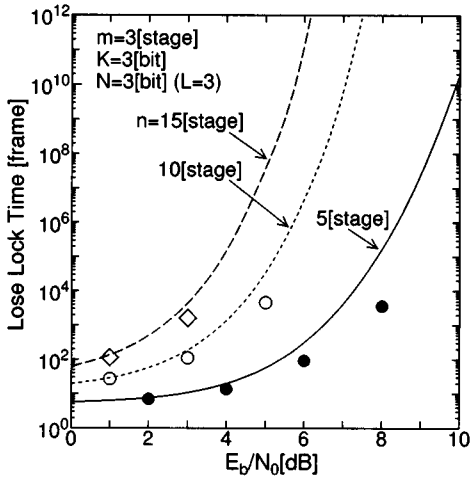

Fig. 6 Lose lock time versus E_b/N_0.

Figure 7 shows the recovery performance when $K=3$ [bit], $N=3$ [bit], $m=3$ [stage], and $n=5$, 10, and 15 [stage]. Each line shows the theoretical value and each plot shows the computer simulation value. The theoretical values agree well with the computer simulation values. The recovery time increases when n is large or $E_b/N_0 \leqq 2$ [dB]. Moreover, the recovery time converges on $(n\times L\times M+1)$ frames when E_b/N_0 increases. Therefore, the recovery times is longer as n increases.

Figure 8 shows the lose lock time and the recovery time for various $m(<n)$, where $K=3$ [bit], $N=3$ [bit], and $n=5$ [stage]. The lose lock time decreases monotonously as m increases. The recovery time increases with increasing m when E_b/N_0 is low, while the recovery time decreases with increasing m when E_b/N_0 is high. It is found that there is the trade-off between the lose lock time and the recovery time.

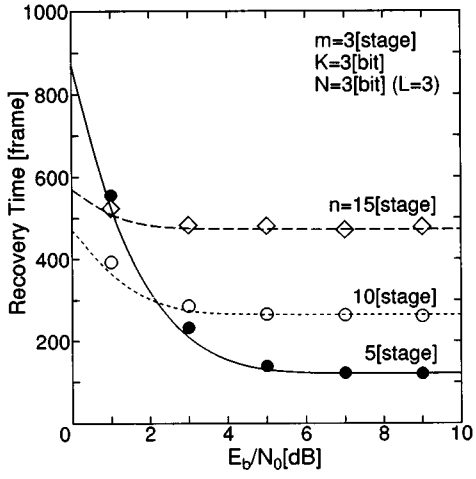

Fig. 7 Recovery performance versus E_b/N_0.

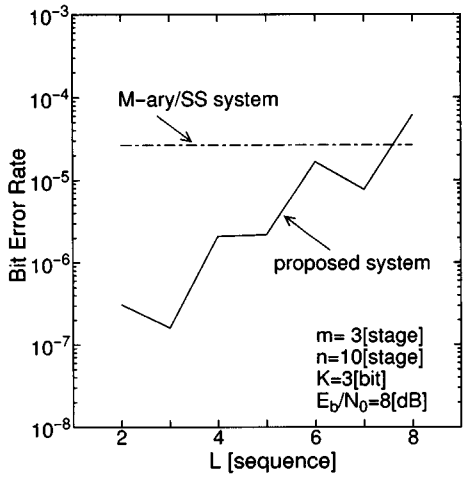

Fig. 9 Constraint length versus BER.

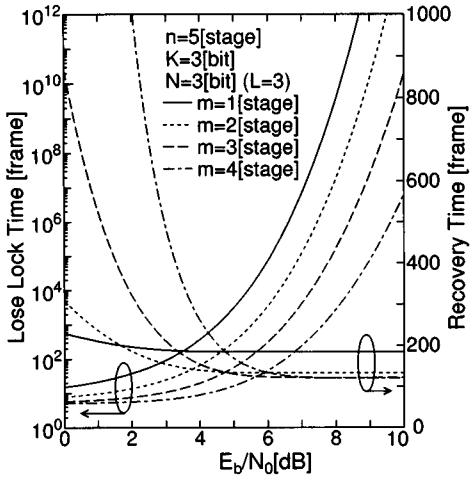

Fig. 8 Lose lock time and recovery time for different values of m where $n = 5$ [stage].

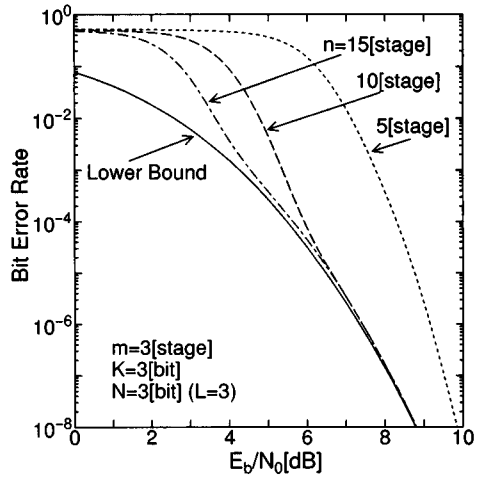

Fig. 10 BER performance considering synchronization performance where $m = 3$ [stage].

Figure 9 shows the constrained length L versus the BER performance considering the synchronization performance when $K = 3$ [bit], $m = 3$ [stage], $n = 10$ [stage] and $E_b/N_0 = 8$ [dB]. The BER is minimum when $L = 3$ [sequence]. Then the BER of the SS-CSC system is better than that of the M-ary/SS system using the proposed synchronization system.

Figure 10 shows the BER performance considering the synchronization performance when $K = 3$ [bit], $N = 3$ [bit] and $m = 3$ [stage].

If n increases, the BER performance considering the synchronization performance can approach the lower bound of the SS-CSC system. The BER performance considering the synchronization performance becomes much the same as the lower bound of the SS-CSC system when $n = 15$ [stage] and $E_b/N_0 \geqq 5$ [dB] or $n = 10$ [stage] and $E_b/N_0 \geqq 7$ [dB].

Figure 11 shows the BER performance considering the synchronization performance for various m, where $K = 3$ [bit], $N = 3$ [bit], and $n = 5$ [stage]. The BER performance improves as m decreases. To approach the lower band, it is necessary to increase n.

5. Conclusions

We proposed the frame synchronization system with the differential detector and racing counters for the SS-CSC system. We described the simple frame synchronization method for the SS-CSC system. Moreover, we discussed the performance. In particular, we evaluated the lose lock time, the recovery time and the BER considering the synchronization performance by theoretical analysis. We obtained the following points.

- The lose lock time decreases when the constraint length L increases. Moreover, increasing n is effective in improvement of lose lock time. And the lose lock time also increases with increasing m, where $m < n$.

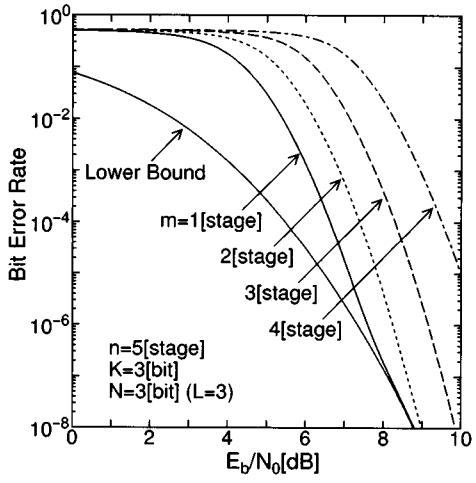

Fig. 11 BER performance considering synchronization performance for different values of m where $n = 5$ [stage].

- The recovery time increases as the constraint length L increases. Moreover, the value of convergence of the recovery time becomes large when n increase. The recovery time increases with increasing m when E_b/N_0 is low, while the recovery time decreases with increasing m when E_b/N_0 is high. It is found that there is the trade-off between the lose lock time and the recovery time.
- The BER performance considering the synchronization performance is minimum when $L = 3$ [sequence]. Then the BER of the SS-CSC system is better than that of the M-ary/SS system using the proposed synchronization system. The BER performance considering the synchronization performance is much the same as the lower bound of the SS-CSC system when $n = 15$ [stage] and $E_b/N_0 \geqq 5$ [dB] or $n = 10$ [stage] and $E_b/N_0 \geqq 7$ [dB].

Future works will include the analysis of chip synchronization.

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